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| <b>FORM PTO-1449</b><br>(Rev. 2-32) | <b>U.S. Department of Commerce</b><br><b>Patent and Trademark Office</b> | <b>Atty. Docket No.</b><br>01-51        | <b>Serial No.</b><br>10/006,516 |
|                                     |  | <b>Applicant:</b><br>Kuang Chi et al.   |                                 |
|                                     |  | <b>Filing Date:</b><br>December 3, 2001 | <b>Group:</b><br>2661           |

**INFORMATION DISCLOSURE STATEMENT BY APPLICANT**  
 (Use several sheets if necessary)

## U.S. PATENT DOCUMENTS

| Examiner Initial | Document Number | Date     | Name          | Class | Subclass | Filing Date if Appropriate |
|------------------|-----------------|----------|---------------|-------|----------|----------------------------|
| QG               | 5 6 0 4 7 7 5   | 02/18/97 | Saitoh et al. | 375   | 376      | 09/29/95                   |
| QG               | 6 1 2 2 3 3 6   | 09/19/00 | Anderson      | 375   | 371      | 09/11/97                   |

## FOREIGN PATENT DOCUMENTS

| Document Number | Date | Country | Class | Subclass | Translation  |    |
|-----------------|------|---------|-------|----------|--|----|
|                 |      |         |       |          | Yes  | No |
|                 |      |         |       |          | <b>RECEIVED</b><br>FEB 15 2002<br>Technology Center 2100 |    |
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|                 |      |         |       |          |  |    |

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

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| QG | PCT Publication No. WO 01/69837 A2, published September 20, 2001, Clock Data Recovery Circuit Associated with Programmable Logic Device Circuitry |
|    |   |
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|--------------------|-----------------|
| EXAMINER           | DATE CONSIDERED |
| <i>[Signature]</i> | 2/23/05         |

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